ABSTRACT OF THE DISCLOSURE

A failure analysis system, includes a chip position calculation module configured to calculate fault chip positions of a plurality of circuit blocks in a chip region based on layout information on the circuit blocks positioned in the chip region and fault information on the circuit blocks; a wafer position calculation module configured to calculate fault wafer positions in a wafer based on the fault chip positions and position information showing a chip region layout in a wafer plane; and a mapping module configured to perform a mapping display of the fault wafer positions in accordance with physical coordinates on the wafer plane.